Demonstration of Low Subthreshold Swing a-InGaZnO Thin Film Transistors
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Abstract
The subthreshold swing is a key parameter in evaluating the power consumption and material properties of the thin film transistors (TFTs). Here we report an amorphous indium gallium zinc oxide (a-IGZO) TFT with a high-$\kappa$ SiO$_2$/HfO$_2$ gate insulator. The device shows a subthreshold swing of 96mV/decade, and an on-to-off current ratio 1.5x10$^{10}$. The low subthreshold swing was attributed to the fully depleted channel state and a low density of mid-gap interface states ($D_{it}$) of 2x10$^{11}$cm$^{-2}$ev$^{-1}$.

INTRODUCTION
Thin film transistors (TFTs) are mainly applied for flat panel displays (FPDs) such as electronic papers (e-papers), organic light-emitting-diodes (OLEDs) and liquid crystal displays (LCDs). To obtain a highly uniform channel layer on such a large substrate, an amorphous phase is required. However, the most conventional hydrogenated amorphous silicon (a-Si) TFTs are insufficient due to the low mobility ($<1$ cm$^2$V$^{-1}$s$^{-1}$). Amorphous indium gallium zinc oxide (a-IGZO), with a relative large electron mobility ($\sim$10 cm$^2$V$^{-1}$s$^{-1}$), may be a promising candidate for next generation FPDs. To reduce the power consumption, fabricating a-IGZO TFTs with low operating voltages and low gate leakage currents is an intriguing topic for researchers in industry and academia. An effective approach to reduce the power consumption is to improve the characteristic of subthreshold swing (SS) and thus shrink the driving voltage range.

We, in this work, introduce a-IGZO TFTs with a high-$\kappa$ SiO$_2$/HfO$_2$ bilayer gate insulator. With efficient modulation of the carriers in the channel, a low SS and a high on-to-off current ratio are achieved. Furthermore, the interface state density ($D_{it}$) was extracted and correlated with the device performance.

EXPERIMENT
The bottom gate a-IGZO TFTs were fabricated on the Corning Eagle 2000 glass substrate. The device fabrication started from depositing the 100nm-thick Mo gate electrode using a DC sputter and patterned by lift-off, and followed by coating a HfO$_2$ gate insulator by ALD (atomic layer deposition) at 280$^\circ$C with a thickness of 35nm. Next, the SiO$_2$/a-IGZO/SiO$_2$ (15nm/50nm/45nm for each layer) tri-layer structure was RF (radio frequency) sputtered at room temperature. The purpose of the sandwiched SiO$_2$ layers is to protect the a-IGZO channel layer from exposure to the air. For the subsequent Mo drain and source contact sputtering, with PR as mask, we then patterned the via holes by reactive ion etching (RIE) with CHF$_3$ gas. Finally, the SiO$_2$ passivation layer was deposited by RF sputtering. The contact pads were then open by RIE with CHF$_3$ gas. Finally, post annealing was performed at 350$^\circ$C under the nitrogen ambient for 30mins.

DISCUSSION
Fig. 2 shows the $I_{DS}$-$V_{DS}$ curves of our a-IGZO TFTs. The gate to source and gate to drain overlap are 5$\mu$m and the corresponding channel width and length are 100 $\mu$m and 3$\mu$m, respectively. A saturation current density of 16mA/mm is achieved when biased at $V_{GS}$=8V and $V_{DS}$=10V. The corresponding transfer characteristics at a $V_{DS}$ of 6V are demonstrated in Fig. 3. Our devices generally show very low hysteresis. As Fig. 3 suggests, the voltage offset is around 50meV. The hysteresis is related to the defect states in the interface of the channel and gate dielectric. Also, the $V_{th}$ (threshold voltage) extracted from the square root of $I_{DS}$ is $-0.87V$. The saturation mobility at $V_{DS}$=6V is calculated to be $\mu_{sat}$=8.9 cm$^2$V$^{-1}$s$^{-1}$ by employing the relative dielectric constants of SiO$_2$/HfO$_2$ bilayer gate insulator, $\kappa$ =3.1, for the gate insulator. The high permittivity of the dielectric layers can effectively increase the amount of the gate-controlled charges $Q_{ox}$ ($=\kappa\varepsilon_0E_{AP}$ where $E_{AP}$ is the applied electric field and $\varepsilon_0$ is the permittivity constant)). Since the carriers in the channel can be effectively modulated by the high-$\kappa$ HfO$_2$ insulator, the current on-to-off ratio reaches 1.5x10$^{10}$. Moreover, the device also exhibits a SS of 96mV/decade. To achieve a low SS, a fully depleted state is preferred [1]. Therefore, two conditions must be required. First, the number of carriers in the channel needs to be less than the maximum oxide controllable charges ($Q_{ox,max}$)

$$qN_{ch} < Q_{ox,max}$$

(1)

Where $t_{ch}$ is the channel thickness and $N_e$ is the carrier density in the channel.

Second, $t_{ch}$ is designed to be less than the width of depletion layer ($W_{dep}$)

$$t_{ch} < W_{dep} = \left(\frac{4\varepsilon_0E_{IGZO}\Phi_b}{qN_e}\right)^{1/2}$$

(2)
Where $\epsilon_{IGZO}=4$ is the relative permittivity constant of a-IGZO, $\phi_0=1.55$V is difference between Fermi level and intrinsic Fermi level ($E_F-E_{Fi}$) in the bulk (the so called bulk potential) [1]. In our case, the a-IGZO channel resistivity was extracted to be $2.8 \times 10^6 \Omega\cdot cm$ by employing TLM (transmission line method) measurement. The corresponding carrier concentration can be obtained following the relation $\rho=q(\mu n)^{\frac{1}{2}}$, where $\mu$ is the mobility, $n$ is the carrier concentration. Assuming $\mu=8.9$ cm$^2$V$^{-1}$s$^{-1}$, which was extracted from the square root of transfer curve in Fig. 3 and was a typical value of amorphous oxide semiconductors [2], the carrier concentration in the channel is $2.5 \times 10^{13}$ cm$^{-3}$. The extracted low carrier concentration is compatible to the extremely high channel sheet resistance ($5.6 \times 10^9$ Ohm/sq, without gate bias) and correspond to an extraordinarily low off current ($\sim 10^{-9}$ mA/mm), which can effectively lower the power consumption of FPDs. For a more conservative evaluation of our carrier concentration, the lower limit of a-IGZO layer mobility can be set to be 1 cm$^2$V$^{-1}$s$^{-1}$ [2] and the corresponding maximum carrier concentration is $2.2 \times 10^{14}$ cm$^{-3}$. In such a case, the carrier concentration is equivalent to a total carrier number of $1.8 \times 10^{20}$ C/cm$^2$, which is much lower than the calculated maximum oxide controllable charges of $2.3 \times 10^7$ C/cm$^2$ at 0.2MV/cm following eq. (1). Furthermore, the depletion width is increased to 2.5µm according to Eq. (2), which is much larger than the channel thickness (50nm). Judging from the considerations above, our device can be fully depleted at the off state, leading to a low SS.

For a-IGZO TFTs, many researchers reported that a higher carrier concentration is desired [2][3] to ensure efficient carrier transport and high operating currents. However, in the case of a-IGZO channel with carrier concentration of $10^{18}$ cm$^{-3}$, the depletion width is around 37nm, which is in the same range of channel thickness. The partially depleted state leads to a larger SS. In this work, by lowering the carrier concentration to the order of $10^{13}$ cm$^{-3}$, the 2.5µm depletion width ensures the fully depleted channel with the design of our layer structure. Despite a low carrier concentration, with a high-$\kappa$ but thin insulator, the carriers are efficiently modulated and a high operating current can still be achieved as is indicated in Fig. 2 and 3.

As the performance of TFTs is close correlated to defect states at the interface of the gate insulator and channel, the CV characteristics of the corresponding MIS (metal-insulator-semiconductor) structure are next investigated. Generally, stretch-out and hysteresis in bidirectional CV characteristics are indicative of fast and slow traps. The former is mainly attributed to interface traps while the latter is to border traps [4]. Fig. 4 illustrates the quasistatic QSCV curves for both sweep directions of our MIS device. The absence of the inversion characteristic is mainly due to the unipolar conduction of a-IGZO channel. During the typical CV measurement which takes a few seconds, the border traps (fixed oxide charge) will exchange charges with the semiconductor layers via tunneling. A small hysteresis of around 40mV implies the excellent quality of our SiO$_2$ insulator. Furthermore, the surface band bending ($\psi_s$) at a given bias ($V_{GS}$) can be calculated following

$$\psi_s (V_{GS}) = \int_{V_{FB}}^{V_{GS}} \left[ 1 - \frac{C_{LF}(V_{GS})}{C_{ox}} \right] dV_{GS}$$

(3)

Where $C_{LF}$ is the low frequency capacitance, which can be measured by QSCV, $V_{FB}$ is the flatband voltage, which corresponds to $V_{GS}$ at the point $C_{LF}$ begins to increase [2]. The inset in Fig. 4 shows that with the increase of ($V_{GS}$-$V_{FB}$), the surface band bending increases rapidly at the beginning and finally saturates.

Fig. 5 shows CV curves at both high and low frequencies. To eliminate the dispersion of HFCV, an improved Two-Frequency method was employed with the frequencies 1MHz and 100kHz selected [5]. Since interface traps can only follow low frequency AC signals, the difference between high and low frequency curves is directly related to the Dit expressed as,

$$D_{it} (V_{GS}) = \frac{C_{ox}}{q} \left[ \frac{C_{LF}(V_{GS})}{C_{ox}} - \frac{C_{HF}(V_{GS})}{C_{ox}} \right]$$

(4)

Since $C_{LF}$ and $C_{HF}$ are functions of $V_{GS}$, the $D_{it}$ versus $V_{GS}$ relation can be calculated from the data in inset of Fig. 4 and Eq. 4. Combining the $\psi_s$ versus $V_{GS}$ relationship, $D_{it}$ is obtained as a function of the energy position in the bandgap and is shown in Fig. 5. Also the results from the conductance method, measured at the frequency range between 1kHz and 1MHz, are shown for comparisons. Due to the small signal to noise ratio, the conductance method allows only a portion of the energy gap, between mid-gap and the Fermi level, to be compared [6]. Both methods agree with each other pretty well within the energy investigated. However, since the equilibrium “frequency” of the quasi static measurement is much lower than the frequencies used by the conductance measurement, the high low frequency CV method can further probe deeper into the bandgap than the conductance method [7]. The $D_{it}$ exhibits a flat value of around $2 \times 10^{10}$cm$^{-2}$ev$^{-1}$ within the bandgap. Near the conduction bandedge, the rapid increase of the interface state density is mainly due to the tail states.

The value of $D_{it}$ at mid-gap is often used as a semiquantitative measure of the macroscopic surface quality. It is reported that the direct deposit of HfO$_2$ on Si results in a high level of $D_{it}$ ($\sim 10^{13}$ cm$^{-2}$ ev$^{-1}$) [8]. A thin SiO$_2$ or SiON buffer layer between high-$\kappa$ and Si interface can reduce the $D_{it}$ to a level between $10^{10}$ cm$^{-2}$ ev$^{-1}$ and $10^9$ cm$^{-2}$ ev$^{-1}$ [8-9]. Also in case of a-IGZO TFTs, it is reported that a high-$\kappa$/a-IGZO interface suffers from larger phonon scattering and
causes an increase of low frequency noise [10]. In our experiment, with a combination of SiO$_2$/HfO$_2$ layer, we exhibit a mid-gap $D_i$ of $2 \times 10^{11}$ cm$^{-2}$ ev$^{-1}$ (from the MIS structure), which is compatible with conventional Si based MOSFET (on the MIS structure) [8-9]. Due to the low $D_i$ and border traps, our a-IGZO TFT shows an excellent SS, a high on to off ratio, and a high saturation current.

CONCLUSIONS

A bilayer high-$\kappa$ gate insulator is employed in the a-IGZO TFT fabricated on the glass substrate. The device demonstrates SS of 96 mV/decade and on-to-off current ratio up to $1.5 \times 10^{10}$. The low SS is attributed to the high-$\kappa$ insulator and the fully depleted channel at the off state, which increase the maximum oxide controllable charges and extend the depletion width. At last, the extracted mid-gap $D_i$ of $2 \times 10^{11}$ cm$^{-2}$ ev$^{-1}$ is compatible with conventional Si based MOSFET, suggesting the high performance of TFTs using a bilayer high-$\kappa$ SiO$_2$/HfO$_2$ gate insulator.
REFERENCES


Fig. 6. The extracted interface state density of a MIS structure using high low frequency method and conductance methods.