Demonstration of Low Subthreshold Swing a-InGaZnO Thin Film Transistors
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Keywords: Amorphous IGZO, Subthreshold Swing, TFTs

Abstract
The subthreshold swing is a key parameter in evaluating the power consumption and material properties of the thin film transistors (TFTs). Here we report an amorphous indium gallium zinc oxide (a-IGZO) TFT with a high-κ SiO2/HfO2 gate insulator. The device shows a subthreshold swing of 96mV/decade, and an on-to-off current ratio \(1.5 \times 10^{10}\). The low subthreshold swing was attributed to the full depleted channel state and a low mid-gap interface state (Dit) of \(2 \times 10^{11} \text{cm}^{-2} \text{eV}^{-1}\).

INTRODUCTION
Among various oxide semiconductors, amorphous indium gallium zinc oxide (a-IGZO) is the most promising candidate for electronic and optoelectronic applications. To lower the power consumption, fabricating a-IGZO TFTs with low operating voltages and gate leakage currents is the topic intriguing to researchers in the industry and academia. An effective approach to reduce the power consumption is to improve the characteristic of subthreshold swing (SS) and thus shrink the driving voltage range.

We, in this work, introduce a-IGZO TFTs with a high-κ SiO2/HfO2 bilayer gate insulator. With efficient modulation of the carriers in the channel, a low SS and a high on-to-off current ratio are achieved. Furthermore, interface state density (Dit) was extracted to correlate the device performance.

EXPERIMENT
The bottom gate a-IGZO TFTs were fabricated on the Corning Eagle 2000 glass substrate. The device fabrication started from depositing the patterned 100nm-thick Mo gate electrode using a DC sputter, and followed by coating a HfO2 gate insulator by ALD (atomic layer deposition) at 280°C with a thickness of 35nm. Next, the SiO2/a-IGZO/SiO2 (15nm/50nm/45nm for each layer) tri-layer structure was RF sputtered at room temperature (RT). The purpose of the sandwiched SiO2 layers is to protect the a-IGZO channel layer from exposing to the air. We then opened via holes by reactive ion etching (RIE) for the subsequent Mo drain and source contact sputtering. Finally, the SiO2 passivation layer was deposited by RF sputtering. The contact pads were then open by RIE. Finally, post annealing was performed at 350 °C under the nitrogen ambient for 30mins. The channel width and length is 150 and 3μm, respectively.

DISCUSSION
Fig. 2 shows the \(I_{DS}-V_{DS}\) curves of our a-IGZO TFTs. A saturation current density of 16mA/mm is achieved when biased at \(V_{GS}=8\text{V}\) and \(V_{DS}=10\text{V}\). The corresponding transfer characteristics at the \(V_{DS}\) of 6V are demonstrated in Fig. 3. Generally, our devices show very low hysteresis. As Fig. 3 suggests, the voltage offset is around 50meV. The hysteresis is related to the defect states in the interface of the channel and dielectric. Also, the \(V_{th}\) (threshold voltage) extracted from the square root of \(I_{DS}\) is +0.87V. The saturation mobility at \(V_{DS}=6\text{V}\) is calculated to be \(\mu_{sat}=8.9 \text{cm}^2\text{V}^{-1}\text{s}^{-1}\) by employing the relative dielectric constants of SiO2/HfO2 bilayer gate insulator, \(\kappa=13.1\), for the gate insulator. The high permittivity of the dielectric layers can effectively increase the amount of the gate-controlled charges \(Q_{ox}\) (=\(\kappa\varepsilon_0E_{AP}\)) (where \(E_{AP}\) is the applied electric field and \(\varepsilon_0\) is the permittivity constant). Since the carriers in the channel can be effectively modulated by the high-κ HfO2 insulator, the current on-to-off ratio reaches \(1.5 \times 10^{10}\). Moreover, the device also exhibits a SS of 96mV/decade. To achieve a low SS, a fully depleted state is preferred [1]. Therefore, two conditions must be required. First, the number of carriers in the channel needs to be less than the maximum oxide controllable charges \(Q_{ox,\text{max}}\)

\[qN_{th}t_{ch} < Q_{ox,\text{max}}\]  \[(1)\]

Where \(t_{ch}\) is the channel thickness and \(N_{th}\) is the carrier density in the channel.

Second, \(t_{ch}\) is designed to be less than the width of depletion layer \(W_{dep}\)

\[t_{ch} < W_{dep} = \left\{ \frac{4\varepsilon_0\varepsilon_{IGZO}\phi_b}{qN_{th}} \right\}^{1/2}\]  \[(2)\]

Where \(\varepsilon_{IGZO}\) is the relative permittivity constant of a-IGZO, \(\phi_b\) is difference between Fermi level and intrinsic Fermi level. In our case, the a-IGZO channel resistivity was extracted to be \(2.8 \times 10^4 \Omega\text{cm}\) by employing TLM (transmission line method) measurement. The corresponding carrier concentration can be obtained following the relation \(\rho=(q\mu)n)^{1/2}\), where \(\mu\) is the mobility, \(n\) is the carrier concentration. Assuming \(\mu=8.9 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}\) as...
was extracted from the transfer curve in Fig. 3, the carrier concentration \( n \) in the channel is \( 2.5 \times 10^{13} \text{ cm}^{-3} \). For a more conservative evaluation of our carrier concentration, the lower limit of a-IGZO layer mobility can be set to be 1 \( \text{cm}^2\text{V}^{-1}\text{s}^{-1} \) and the corresponding maximum carrier concentration is \( 2.2 \times 10^{14} \text{ cm}^{-3} \). In such a case, the carrier concentration is equivalent to a total carrier number of \( 1.8 \times 10^{10} \text{ C/cm}^2 \), which is much lower than the calculated maximum oxide controllable charges of \( 2.3 \times 10^{-7} \text{ C/cm}^2 \) at 0.2MV/cm following eq. (1). Furthermore, the depletion width is increased to 2.5μm according to Eq. (2), which is much larger than the channel thickness (50nm). Judging from the considerations above, our device can be fully depleted at the off state, leading to a low SS.

For a-IGZO TFTs, many researchers reported that a higher carrier concentration is desired [2][3] to ensure efficient carrier transport and high operating currents. However, in the case of a-IGZO channel with carrier concentration of \( 10^{18} \text{ cm}^{-3} \), the depletion width is around 37nm, which is in the same range of channel thickness. The partially depleted state leads to a larger SS. In this work, by lowering the carrier concentration to the order of \( 10^{14} \text{ cm}^{-3} \), the 2.5μm depletion width ensures the fully depleted channel with the design of our layer structure. Despite a low carrier concentration, with a high-\( \kappa \) but thin insulator, the carriers are efficiently modulated and a high operating current can still be achieved as is indicated in Fig. 2 and 3.

As traps in the material structure are critical to the performance and reliability of the thin film transistors, \( D_{it} \) was extracted from a MIS (metal-insulator-semiconductor) capacitor by high low frequency and conductance methods. Both methods agree with each other pretty well within the energy investigated. The extracted low mid-gap \( D_{it} \) of \( 2 \times 10^{11} \text{ cm}^{-2}\text{eV}^{-1} \) suggest that a bilayer high-\( \kappa \) SiO\(_2\)/HfO\(_2\) may be a promising gate insulator for amorphous oxide semiconductors.

**CONCLUSIONS**

A bilayer high-\( \kappa \) gate insulator is employed in the a-IGZO TFT fabricated on the glass substrate. The device demonstrates SS of 96 mV/decade and on-to-off current ratio up to \( 1.5 \times 10^{10} \). The low SS is attributed to the high-\( \kappa \) insulator and the fully depleted channel at the off state, which increase the maximum oxide controllable charges and extend the depletion width. At last, the extracted mid-gap \( D_{it} \) of \( 2 \times 10^{11} \text{ cm}^{-2}\text{eV}^{-1} \) is compatible with conventional Si based MOSFET, suggesting the high performance of TFTs using a bilayer high-\( \kappa \) SiO\(_2\)/HfO\(_2\) gate insulator.

**REFERENCES**


Fig. 4. The extracted interface state density of a MIS structure using high low frequency method and conductance methods.