Engineered Substrates: Alternative Technologies Using Materials Integration

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Abstract

Two issues related to fabrication of engineered substrates will be discussed. First, the transfer of III-V template layers to alternate substrates layers will be described with special emphasis on issues related to costs associated with the technology.

A second issue is the development of porous semiconductors for subsequent epitaxial growth and device layer transfer. There is great potential in porous III-V materials with the concomitant high substrate costs or the requirement to transfer device layers to, for example, flexible substrates. The development of porous layers using InP requires the ability to control the mechanical properties of the porous layers, and ability to transfer the epitaxial layers deposited on the porous layers to different substrates.

INTRODUCTION

With the continuing advances in III-V based devices, there is increasing interest in techniques to promote the transfer of the device layers to alternative substrates. The origins are twofold. First, there is an economic advantage to limit the use of III-V substrate material. For example, a thin (~ 1 μm) template layer of the III-V material on a low cost substrate (silicon or a polycrystalline material) allows, for example, for a 300 μm thick III-V substrate to be sliced into many 1 μm slices. This may be important for the final cost of a high efficiency multi-junction III-V photovoltaic (PV) cell since the substrate represents about one third of the total cost while the cost of a silicon substrate is a very small fraction of the processing costs involved in integrated circuits. The reduction of the use of the substrate material in the fabrication of the final device in the case of high efficiency PV cells would make them more cost-competitive with other technologies. Additionally, the development of inverted metamorphic structures for high efficiency PV cells requires that the original growth substrate be removed. Presently, this is accomplished by grinding or etching the original substrate whereas the use of alternative technologies may prove to be more effective. For situations where layer transfer is touted as a means to better cost effectiveness, the cost of the transfer process must be considered against the cost of the original substrate.

Improved performance is a second area in which alternative substrates are relevant. This is the case for silicon-on-insulator In III-V systems, for example, the performance of high power III-V transistors improves with better heat dissipation from the junction. This can be accomplished with the use of high thermal conductivity materials; ideally the integration of a high thermal conductivity material such as diamond with the III-N device would provide a superior combination.

In many cases, the utilization of layer transfer and materials integration may include both an economic advantage and also a performance advantage. Two separate approaches are addressed to achieve these advantages. The first involves the production of a substrate in which a thin template or laminate of the material with the correct lattice parameter is bonded to a separate substrate. This composite structure is then used for the subsequent epitaxial deposition of the device layers. This approach is the exemplified by the commercially available silicon-on-insulator structures in which a thin (~ 1 μm) silicon template is stacked on an oxide layer on a second silicon substrate. We have extended that approach by stacking a thin (~ 1 μm) III-V template layer such as GaAs, InP or GaN onto a dielectric layer which is, in turn, deposited on a different substrate, such as silicon, GaAs, or a polycrystalline material. In the scientific literature, we addressed many of the components necessary to produce these structures for a variety of III-V materials, namely the fundamental issues for the transfer of a μm-thick layer through hydrogen implantation and exfoliation via post-implant annealing[1], the ability to bond the III-V layer to an alternative substrate through a dielectric layer[2] [3] (and more recently, the ability to bond III-V wafers to produce a highly conductive interface[4] although that is not a main thrust here), the chemical mechanical polishing to achieve low overall removal rates while achieving planar, damage-free surfaces and the epitaxial deposition of device layers on these composite substrates,[5] and an understanding of the limitations of this approach, specifically related to the differences in the coefficients of thermal expansion among the device layers, the template layer, and the underlying substrate.[6]

In this work, we describe efforts to reduce the costs that are associated with the layer transfer process. The key cost...
is the hydrogen (or other light ion) implant; the high price reflects the fact that a dose of greater than ~5x10^{16} \text{cm}^{-2} is necessary. Typically, the implant is hydrogen, the energy is \sim 160 \text{keV}, although both parameters are target (wafer) dependent and energy (depth) dependent. An approximate cost for this implant (by a commercial implant house) over a 100 mm diameter wafer is about $1,000. Certainly, there will be cost reductions for larger quantities, but the key point is that the implantation step is not inexpensive. If the layer transfer leads to improved performance, then the cost may not be such a key factor; however, if cost reduction is the key or the logic is that generating multiple thin slices from a single wafer will lower costs, then the cost of the implant compared to the cost of the original wafer is important. However, by adding a relatively low dose of He (5x10^{15} \text{cm}^{-2}), the dose of hydrogen can be reduced by about a factor of two, significantly reducing the cost of implantation (which is nominally proportional to the dose). This approach points to the importance of implantation techniques that are lower cost than tradition implantation processes.

The second overall approach employs the use of a mechanically weak porous layer upon which the device layers are epitaxially grown. This approach also has its origin in a silicon-based process in which epitaxial silicon layers are grown on a porous silicon layer and later transferred to a separate substrate through the mechanical fracture of the porous layer.[7] We have extended this idea by transferring an InP template layer to a porous silicon / silicon substrate (Cleave-Engineered Layer Transfer (CELT))[8, 9], grew InP epitaxy on the layer and transferred the template and epitaxial layer to an alternate (glass) substrate. It is important to understand how the porosity changes during annealing / subsequent epitaxial growth such that the porous layer is sufficiently strong to withstand the epitaxial deposition process but weak enough to achieve facile fracture during the subsequent transfer process.[10] A more direct approach is the direct growth of a III-V device structure on a porous III-V layer; we address our initial efforts in the formation of porous III-V in which the mechanical properties can be controlled to split off the upper layer (as well as any epitaxy deposited on it). The relationship between the porosity and mechanical properties is an important engineering parameter.

**Fabrication**

**A) Hydrogen Dose Reduction**

To address the costs associated with the implantation process, GaAs substrates were implanted with different doses of hydrogen and helium. 50 and 100 mm diameter SI GaAs substrates with SiN dielectric coating (80 nm) were subject to the implant conditions listed in Table 1. For these implant conditions, the projected range of the He^+ and the H^+ is approximately 0.7 \mu m. The annealing conditions are meant to enhance bonding and initiate the nucleation of the hydrogen platelets at \sim 150 °C and then to grow the hydrogen platelets that produce the exfoliation at 300 °C. Next, after the exfoliation annealing conditions were determined for the different implants, a second set of wafers was bonded to separate wafers (either GaAs or silicon), annealed at 150 -200 °C to promote bonding and then ramped up to 300 °C to induce exfoliation. CMP using NaOCl and C_6H_8O_7 was performed to produce a surface that is suitable for subsequent epitaxial deposition.

<table>
<thead>
<tr>
<th>Dose (\text{cm}^{-2})</th>
<th>Temperature (°C)</th>
<th>Energy (keV)</th>
</tr>
</thead>
<tbody>
<tr>
<td>H: 1x10^{17}</td>
<td>-20</td>
<td>80</td>
</tr>
<tr>
<td>H: 6x10^{16}</td>
<td>-20</td>
<td>80</td>
</tr>
<tr>
<td>He: 5x10^{15}</td>
<td>-20</td>
<td>105</td>
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<tr>
<td>H: 4x10^{16}</td>
<td>-20</td>
<td>80</td>
</tr>
<tr>
<td>He: 5x10^{15}</td>
<td>-20</td>
<td>105</td>
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<tr>
<td>He: 5x10^{15}</td>
<td>-20</td>
<td>105</td>
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Table 1. Implant parameters for reduced cost GaAs layer transfer

**B) Porous Layer Formation**

Porous InP layers were produced using anodic etching in a manner similar to the porous silicon. P-type wafers were used in a 5% HCl aqueous solution in which anodic etching of the substrate took place under different current densities and times, to control the porosity and porous layer thickness. Typical current densities were 25-100 mA/cm² and etch times were 15-120 seconds.

**Results and Discussion**

**A) Hydrogen Dose Reduction**

X-ray diffraction scans represent an important metric to understand the exfoliation process of light ion implanted semiconductors. The figure below shows the (004) diffraction scans from the wafers that were subjected to the different implant conditions. The strain-induced fringe pattern stems from the implantation process and the sharp fringes indicate that the implant species have not migrated significantly during the implant. The scans also show that the maximum strain in the layer – represented by the left peak – includes the implanted species and defects created during the implant process. The helium introduces strain on the same order as the hydrogen, even though the concentration is approximately one order of magnitude less. Given that the cost to implant a 100 mm diameter wafer to these doses is approximately $1,000 for the hydrogen, and $200 for the helium, the ability to replace the hydrogen with helium would represent a significant cost savings.

After the annealing sequence, each of the structures exhibits similar behavior: the strain-related peaks shift toward the substrate peak, which indicates a decrease in the strain present. This has been shown[11] to result from the agglomeration of hydrogen and point defects into the platelet structures that cause the exfoliation. In this case, we employed a lower temperature anneal (150 – 200 °C) for several hours followed by a short (few minutes) anneal at 300 °C. The addition of helium appears to provide a highly strained region at which the hydrogen can agglomerate and
thus promote exfoliation. For this series of implant and annealing conditions, a successful implant and anneal process is achieved with the hydrogen implant reduced from $1 \times 10^{17}$ cm$^{-2}$ to $6 \times 10^{16}$ cm$^{-2}$ with the addition of $5 \times 10^{15}$ cm$^{-2}$ helium. In comparison, a GaAs substrate implanted with $6 \times 10^{16}$ cm$^{-2}$ hydrogen without the helium co-implant does not exhibit exfoliation; therefore, the helium co-implant promotes hydrogen platelet formation and aids in layer transfer at lower overall implant doses.

Using these parameters, GaAs was bonded to a separate substrate (Si in this case), and annealed under the same combination of annealing conditions and doses. The figure below shows a scanning electron microscopy (SEM) cross section of the exfoliated layer from a 100 mm diameter GaAs substrate that is transferred to a new substrate. The roughness at the surface is due to the exfoliation step. After a CMP step using NaOCl and C$_6$H$_8$O$_7$ which removes approximately 0.1 – 0.2 μm, the surface is suitable for subsequent epitaxial deposition.

These results point toward the direction that is necessary for light ion implantation to be successfully incorporated: the implant costs must be reduced to make the process more economically viable. Here, a co-implant process has been shown to help achieve this goal. Further developments may include the use of plasma immersion ion implantation or other less precise implant processes combined with a lower dose / high strain implant (such as with He in this case).

Using the etching conditions of a 5% HCl solution and current densities in the 25-100 mA/cm$^2$ range, the InP is expected to exhibit a porous structure that is aligned along the (111) crystallographic planes. In fact, this alignment is readily observed for all of these samples as shown in the figure below for the sample etched under 25 mA/cm$^2$ and for 60 s. The crystallographic nature of the porous layer is readily observed.

Nanoindentation results demonstrate that the porous nature of the film reduces the modulus by up to 75% depending on...
the porosity in a manner similar to what was observed in the nanoindentation of porous silicon.[8]

Based on the results, it was possible to controllably change the current density during the etching cycle to produce a more porous deeper layer and a denser surface layer. This double-porous structure is expected to promote fracture in the more porous layer and allow for the transfer of the top layer (along with the epitaxial layers deposited on the porous layer).

This controlled fracture is demonstrated by a double-etch process followed by the application of force at the porous InP – InP interface to mechanically separate the top, denser porous layer from the substrate with fracture at the more porous interfacial layer. The porous layer does indeed delaminate and is removed from the substrate. This is shown in the figure below in which a portion of the delaminated top InP layer is resting on the remaining substrate.

**Figure 5.** Delaminated top porous InP layer after mechanical removal from the remainder of the substrate. The top layer is about 1 μm thick. The fracture plane that corresponds to the more porous underlying layer is clearly visible at the bottom of the image.

This result is extremely promising for the development of epitaxial layer transfer based on the formation of mechanically weak porous III-V layers via electrochemical etching.

**CONCLUSIONS**

III-V engineered substrates continue to evolve. The use of co-implants such as relatively low doses of helium promote exfoliation at lower hydrogen doses, which reduces the overall cost of the layer transfer process. Porous III-V layers – here InP – are advanced as another CELT substrate through which the introduction a mechanically weak layer for the subsequent layer transfer has been achieved.

**ACKNOWLEDGEMENTS**

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**REFERENCES**


**ACRONYMS**

CMP: Chem-Mechanical Polishing
SEM: Scanning Electron Microscopy
CELT: Cleave Engineered Layer Transfer

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