

## **SESSION 15: BACKSIDE PROCESSING**

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For years there have been backside processing sessions at ManTech. In earlier years it was GaAs then we had a brief flutter of papers relating to InP and last year we had several papers on SiC. This year's backside session has a balance between GaAs and SiC.

The session begins with an exciting paper from Fujitsu Limited and Fujitsu Laboratories Ltd. The paper discusses the process issues relating to the wafer support for SiC via etching and wafer dicing for GaN HEMT MMICs with 0.1 $\mu$ m length gates and a very thin SiN passivation layer. The second paper is a joint paper from United Monolithic Semiconductors and Fraunhofer Institute for Reliability and Microintegration. A Mobile Electrostatic Carrier (MEC) for the temporary bonding of thin GaAs wafers using an electrostatic force for processing and handling in a manufacturing area will be presented. The next paper comes from TriQuint Semiconductor in Texas and reviews the effects of the various process parameters on pillar formation in SiC vias. Optimised process conditions will demonstrate a SiC backside via manufactured at relatively low temperatures. The final paper in this session comes from Mitsubishi Electric Corporation and investigates the use of Ni-P as a seed layer prior to Au plating. The Ni-P causes stresses in the wafer. This paper will show the causes of this stress and a process that has been introduced to reduce it.