

# 0.15 Micron Gate 6-inch pHEMT Technology by Using I-Line Stepper

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## Abstract

**A production ready 0.15 $\mu$ m-optical-gate pseudomorphic high electron mobility transistor (pHEMT) using i-line stepper has been developed. Yield exceeding 99% is demonstrated for devices with 0.9mm gate width across a 6-inch GaAs wafer. These results indicate that the 0.15 $\mu$ m optical gate pHEMT technology is ready for high volume production with low cost at WIN Semiconductors.**

## I. Introduction

Traditionally 0.15  $\mu$ m gate has been achieved using e-beam direct write.<sup>[1]</sup> However, an E-beam direct write tool is very expensive with very limited throughput. Hence in recent years, 0.15  $\mu$ m gate has been realized using dielectric assist approach.<sup>[2]</sup> This approach is either with high level of complexity and or relatively high associated cost. In this paper, we will report the successful development of a low cost and production worthy, 0.15  $\mu$ m power pHEMT using i-line stepper without using the dielectric assist approach.<sup>[3]</sup>

## II. Epi Structure and Process

- Epi

WIN 0.15 $\mu$ m optical-gate pHEMT devices utilize molecular beam epitaxy (MBE) grown material on 6-inch GaAs substrate. The pHEMTs consist of double side doping to achieve high current density. The cross section of a 0.15 $\mu$ m gate-width device is sketched in Figure 1. The epi structure consists of a thin, undoped InGaAs channel layer, with high indium concentration. Double delta-doped layers provide carriers to the channel. The front to back pulse dope ratio is 2.5. AlGaAs spacer layers are grown between the channel layer and the Si pulse-

doped layers. An AlGaAs Schottky layer is placed on top of the upper spacer layer.

- Process

For device processing, the 0.15 $\mu$ m optical-gate process flow is listed in Table 1. Ohmic patterns are defined by stepper lithography and Au/Ge/Ni/Au metals are evaporated in the contact regions in order to have good ohmic contact, and sintering is performed using rapid thermal annealing with optimized conditions. Low contact resistance ( $R_c$ ) of 0.1 $\Omega$ -mm is achieved.

After Ohmic alloy, the 0.15  $\mu$ m gate is defined by sequential construction with two different resist materials. As shown in Figure 2, the first resist forms a trench directly over GaAs substrate. The i-line stepper then exposes this resist at a certain dimension. This resist is then developed and reflowed thermally to have the trench uniformly shrunk down into a 0.15 $\mu$ m slit as required. The second resist is then applied to define the overhang of the T-shape. The gate recess profile is controlled by wet-etch process. The gate level is completed by Ti/Pt/Au evaporation. Thus, this "T" gate metal technology can ensure a low gate resistance. Figure 3 shows the SEM cross-section picture of WIN 0.15 $\mu$ m optical gate.

After the gate definition, the device is fully passivated by SiN of 1000 $\text{\AA}$  thick. Resistors are provided using both epitaxial layers and TaN thin films. The TaN resistor with sheet resistance  $50 \pm 1 \Omega/\text{sqr}$  is fabricated. The MIM capacitor has a capacitance of  $600 \pm 60 \text{ pF}/\text{mm}^2$ . As shown in Figure 4, air bridges with 4- $\mu$ m plated Au produce minimal interconnect capacitance. Optional BCB and protection silicon nitride layers provide handling

robustness. Wafers are thinned to either 100 or 50 $\mu\text{m}$  for improved thermal and RF performance.

The summary of process characteristics is listed in Table 2.

- Gate Yield

The excellent yield and reproducibility are mainly related to the well controlled gate photo lithography process. Gate yield of each wafer is evaluated using 12x75  $\mu\text{m}$  devices. Our spec is 0.05mA/mm in drain current defined at grounded source, -2V gate bias and 1.5V drain bias. Figure 5 demonstrates 99.2% of 188 12x75  $\mu\text{m}$  devices across 6-inch GaAs wafer show normal FET characteristics with satisfactory drain current pinch off. These results show that WIN 0.15 $\mu\text{m}$  pHEMT process is ready for production of high volume MMIC.

### III. Device Performances and Characteristics

- DC & RF

The typical transfer curve is presented in Figure 6 and Table 3. An extrinsic transconductance of 690mS/mm, Ron of 1.2 $\Omega$ -mm, and Vto of -0.3V with an  $f_t$  of 92.0GHz is routinely achieved on 6" GaAs substrates. The drain current density (IDSS) at VGS=0V is 80mA/mm, and the saturation drain current density (Idmax) at VGS=0.5V and VDS=1.5V, is 410mA/mm. The typical drain-to-gate breakdown voltage VDG is 11.5V. This is defined at Ig=1mA/mm.

The uniform  $f_t$  and  $f_{\text{max}}$  across 6-inch GaAs wafer are demonstrated in Figure 7 and Figure 8, respectively. The typical  $f_{\text{max}}$  is around 209 GHz.

- Power Performance

Figure 9 demonstrates the loadpull measurements of an 2x75 $\mu\text{m}$  device taken at 29GHz with VDS=3.5V, 133mA/mm IDS. Psat of 17.3dBm (361mW/mm) with maximum PAE of 44.0% and linear gain of 13.9dB is provided. The P1dB is around 16.5dBm (301mW/mm) at VDS=3.5V.

- Noise Performance

The Ku-version pHEMT provides a 1.59dB noise figure as well as 7.84dB associated gain at 40GHz. The pHEMT is biased at 1.8V and draws 50mA/mm IDS current during operation, as shown in Figure 10.

### IV. Summary and Conclusions

A cost-effective and excellent performance WIN 0.15 $\mu\text{m}$  power pHEMT process is presented in this paper.

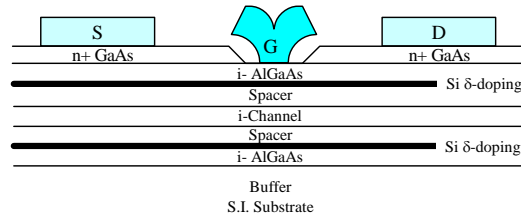


Figure 1. Cross section of WIN 0.15 $\mu\text{m}$  optical-gate pHEMT device.

Table 1. The 0.15 $\mu\text{m}$  optical-gate pHEMT process flow.

Step	Name	Description
1	Ohmic	Ohmic Metal and Alignment Key
2	Mesa	Mesa Implant
3	Ogate	Optical Gate
4	DRES	Dual Resist
5	Via1	First Nitride Deposition, Via Etch
6	TFR	Thin Film Resistor
7	Met1	First Interconnect Metal
8	Via2	Second Nitride Deposition, Via Etch
9	Span	Span
10	Met2	Second Interconnect Metal
11	Backvia	Backside Via
12	Street	Backside Street

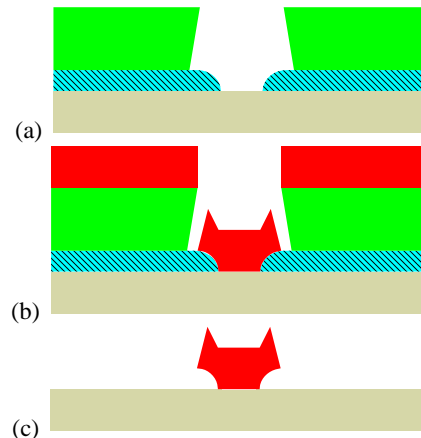


Figure 2. The i-line 0.15 $\mu\text{m}$  optical gate process.

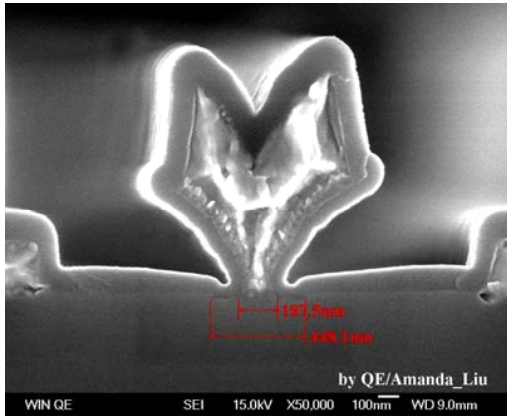


Figure 3. SEM cross section of WIN 0.15µm optical gate.

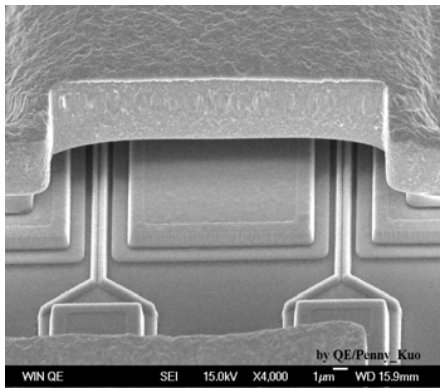


Figure 4. Air bridges with 4-µm plated Au produce minimal interconnect capacitance.

Table 2. The 0.15µm optical-gate pHEMT process Characteristics.

Item	Characteristics
Backside via size (µm <sup>2</sup> )	30 x 60
Gate length (µm)	0.15
Gate metal thickness (µm)	0.6
Interconnect metal layer	2
Metal 1 thickness (µm)	1.1
Metal 2 thickness (µm)	4
Thin film resistor (ohm/sq)	50
MIM capacitor (pF/mm <sup>2</sup> )	600 or 400

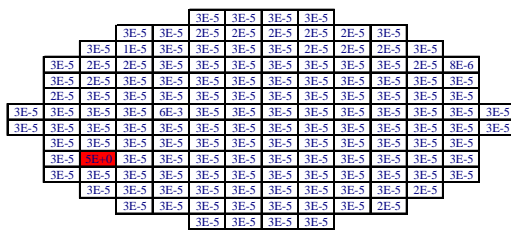


Figure 5. 99.2% of 188 instances of 12x75 µm devices across 6-inch GaAs wafer show normal FET characteristics with satisfactory drain current pinch

off. Our spec is 0.05mA/mm in drain current defined at grounded source, -2V gate and 1.5V drain bias.

Table 3. Typical values of DC device parameters measured on a single finger FET.

Parameter	Symbol	Unit	Value
Extrinsic transconductance	GM_PEAK	mS/mm	690
Maximum drain current @ Vgs=0.5V, Vds=1.5V	Idmax	mA/mm	410
Drain current @ Vgs=0V, Vds=1.5V	IDSS	mA/mm	80
On resistance @ Vgs=0.5V	RON	Ohms*mm	1.2
TLM epi sheet resistance	RS_TL_EP	Ohm/sq	140
Gate-drain breakdown @ Igd=1mA/mm	VDG	V	11.5
Pinch-off voltage @ Ig=1mA/mm	Vto	V	-0.3
Cut-off frequency @ Vds=1.5 volt	ft	GHz	92.0

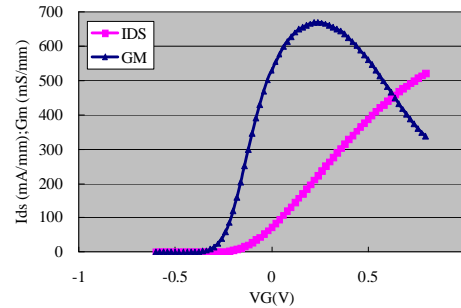


Figure 6. The transfer curve of WIN 0.15µm pHEMT 2x75µm device

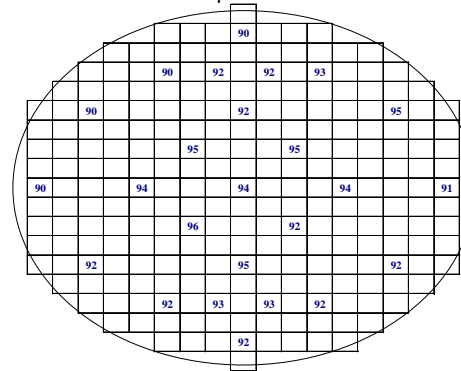


Figure 7. The typical ft is around 92 GHz. The uniform ft across 6-inch GaAs wafer demonstrates WIN 0.15µm optical gate is repeatable with high yield.

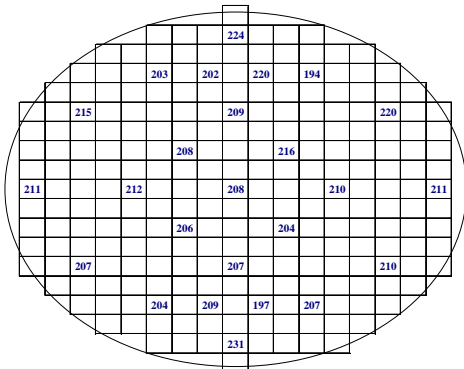


Figure 8. The typical  $f_{max}$  is around 209 GHz. The uniform  $f_{max}$  across 6-inch GaAs wafer demonstrates WIN 0.15 $\mu$ m optical gate is repeatable with high yield.

- [2] Andrew T. Ping et al., "A High-Performance 0.13- $\mu$ m AlGaAs/InGaAs pHEMT Process Using Sidewall Spacer Technology" 2005 GaAs MANTECH Technical Digest.
- [3] Cheng-Guan Yuan et al., "Quarter-Micron Optical Gate 6" Power pHEMT Technology," APMC2008 Proceedings.

### Acronym

- 1. pHEMT: pseudomorphic high electron mobility transistor

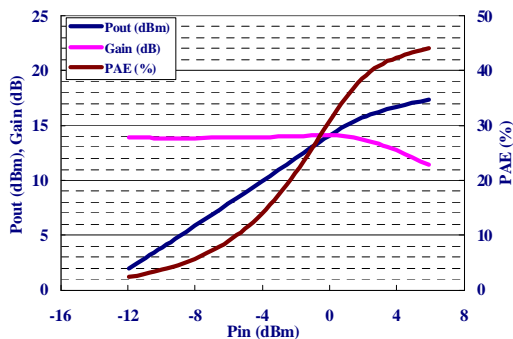


Figure 9. A P1dB power of 16.5dBm (301 mW/mm) with maximum PAE of 44.0% is achieved at 29GHz, 3.5V VDS, 133mA/mm from 2x75 $\mu$ m FET.

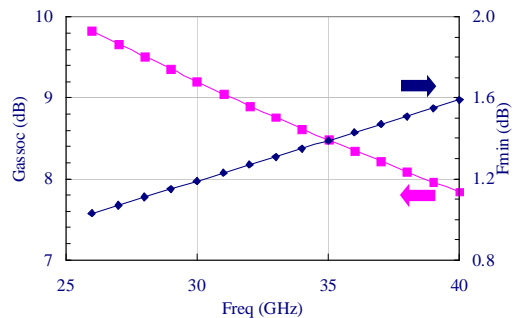


Figure 10. 2x75 $\mu$ m pHEMT device shows 1.59dB  $F_{min}$  and 7.84dB associated Gain at 40 GHz, 1.8V VDS, and 50mA/mm IDS.

### Acknowledgement

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### References

- [1].M. Chertouk et al., "Manufacturable 0.15 mm PHEMT Process for High Volume and Low Cost on 6" GaAs Substrates" 2002 GaAs MANTECH Technical Digest.