

Technological challenges for manufacturing power devices in SiC

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Keywords: Silicon Carbide, MOSFET, JFET, Annealing, Contacts

Abstract

The paper discusses important challenges in manufacturing silicon carbide based power devices on an industrial scale. Special emphasize is paid to processes which differ considerably from well know silicon power device process flows. The main topics discussed in the contribution are processes for annealing ion implanted species, the formation of ohmic contacts as well as the crucial question of forming high quality interfaces between SiC and insulating materials for MOS based power devices structures.

INTRODUCTION

A certain attention paid to wide band gap semiconductors was observed beginning in the early nineties. Regarding power devices, it was focused during the last years to the most interesting materials like GaN and SiC. Especially SiC has realized an impressive growth process due to its remarkable technological advantages. In contrast to the most other candidates among the wide band gap semiconductors SiC can be characterized by the following advantages

- Indirect semiconductor, important for bipolar power electronics e.g.
- Ability for selective doping of both, n- and p-type
- Native thermal oxide SiO₂
- Freestanding and high quality crystals available
- Broad targeted range of applications (power electronics, high frequency electronics optoelectronics, high temperature electronics etc.)

At the moment, unipolar structures like Schottky barrier diodes and FETs are favored for main stream applications. Bipolar structures are expected to be used for very high blocking voltages. The introduction of first products (Schottky barrier diodes) occurred in 2001 by Infineon and Cree. Even considering the higher device price, the implementation in systems could be realized also from an economical point of view due to the achievable system advantages [1]. The use of SiC components is mainly triggered by the possibility to achieve higher power densities for power conversion systems via higher switching frequencies. The now released new generation of Schottky

Barrier diodes represents a next step towards the really ideal power diode [2].

The development of SiC based switching devices is close to a product release. Addressable applications are high voltage applications in energy systems as well as the huge market for low voltage power switches, where even in the blocking voltage range below 100V SiC is assumed to be one potential candidate for meeting the increasing demands on power density [3]. However, especially the complex technology of switching devices represents a challenge for SiC components. Important differences to the established silicon technology exist, and therefore, even if the basic structures look like comparable, remarkable technological efforts are required to establish a working and stable technology flow. The paper will address selected fields of SiC device manufacturing steps and will sketch some possible solutions how to handle it. I the focus will be high temperature aspects as well as new phenomena not known in silicon device processing.

ANNEALING OF ION IMPLANTATIONS

Compared to silicon device processing, especially high temperature treatments during the process flow require new solutions. As an example, the implant annealing has to be performed at temperatures well above 1500°C and thus, close or above the growth temperature of the epitaxial layer. As a result, a serious surface degradation, called step bunching, can be observed (see Fig. 1b). This effect becomes dominant for annealing temperatures above 1500°C. Especially region which have seen ion-implantation are affected, most crucial are p-type implanted regions which form an irregular groove structure compared to non-implanted areas showing lines parallel to the steps given from the off-orientation. Even if it is basically possible to work on these surface, mainly if the device operation is not directly related to the surface morphology like for a JFET with its bulk channel, for several other reasons this surface degradation should be suppressed. Automated pattern recognition for instance needs flat surfaces in order to distinguish the adjustment marks properly. Topologies formed on the surface should remain sharp and not flatten out as usual observed as a result of the step bunching. Finally, for the formation of MOS interfaces at such a

surface, a low roughness is highly appreciated. Since the reason for the degradation is believed to be the loss of silicon from the surface, first solutions were based on adding silicon to the process atmosphere. However, difficulties came up especially assuming batch type processes. Another alternative way presented earlier was short time processing offered by RTP like systems [4], but for using this technology commercially, the equipment needs to be improved for the temperature range above 1500°C. Today the preferred method is to use a so called graphite cap, mostly formed by applying photo resist to the wafer and baking it out as extremely high temperatures.

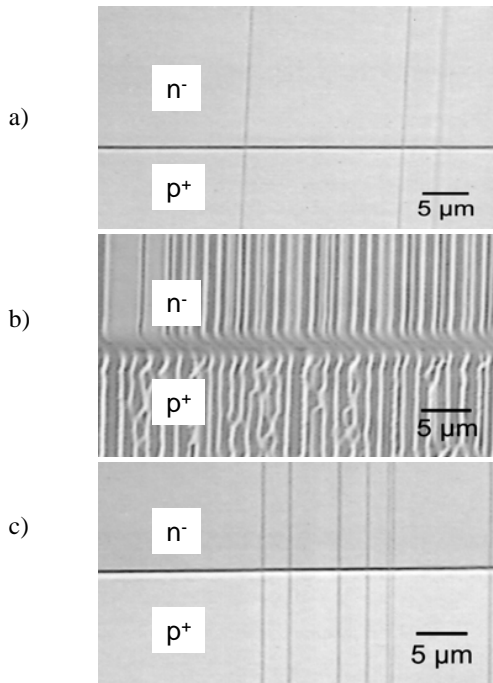


Figure 1 : Surface morphology of SiC, a) before annealing, b) after annealing without surface protection c) after annealing using a graphite cap to prevent step bunching, for every picture the upper part shows a non-implanted region, the lower part a region implanted with aluminum

This cap effectively protects the surface from degradation (see Fig. 1c). Crucial is the proper removal of this layer after the annealing step without affecting the underlying surface. Other cap approaches, using AlN e.g. [5], often require the use of KOH for removal which also etches SiC and thus, are not well suited for device processing.

Another challenge arising from the high annealing temperature is the formation of self aligned MOS devices, e.g. Diffusion cannot be observed in SiC – despite the non controlled behavior of implanted boron. Also using the gate as an implant mask will not work since both, the interfacial oxide layer as well as the gate material will not survive the annealing temperature. Thus, other methods need to be used for forming dense packaged cell devices with a high

precision of the channel length e.g. Mostly spacer techniques are presented today [6], however, this concept has certain limitations regarding the range of addressable dimensions.

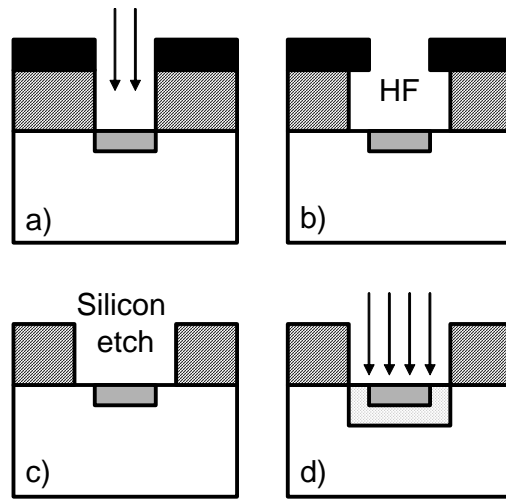


Figure 2 : Method for the precise and self-aligned formation of MOSFET or JFET channels in SiC power devices, a) formation of a double layer mask and first implant (e.g. source), b) under etch using wet oxide etch c) removal of the silicon roof by wet etching d) second implant, e.g. p-well

An alternative concept was developed in our labs [7], using a first double mask layer of oxide covered by polysilicon (see Fig. 2). This double layer will be opened by reactive ion etching with a nearly perfect 90° slope for the sidewalls. Then, a first implantation, e.g. for the source, can be performed. Afterwards, the wafer is placed in to an HF acid fluid and controlled under etching can be realized. The slope of the sidewall remains nearly perfect and under etching up to several μm can be achieved with a precise control in the range of 50nm. After this etching process, the silicon roof can be etched and a new implantation mask with a precise distance to the first implantation exists. The advantage here is that the silicon roof can be removed selectively to the semiconductor by wet processing. Now, the p-type implant for forming the well in MOSFETs e.g. can be added (Fig. 2d).

One of the hurdles for a further progress in annealing processes and the formation of a common understanding and modeling is definitively the lack of commercial equipment. First reactors appear meanwhile on the market; however, still a breakthrough is not visible regarding this topic.

OHMIC CONTACTS

Ohmic contacts can be formed only by sintering refractory metals at temperatures well above 800°C, what implies that the contact formation is in between the process and not a final step like in silicon technology. As an example, a Schottky barrier can only be formed with an existing ohmic contact at the backside, limiting the applicable processes

because of metal components at the wafer. Ohmic contacts to SiC are predominantly formed by using nickel based layers. In general, high impurity concentrations well above $5 \times 10^{18} \text{ cm}^{-3}$ are required. For contacting n-type layers, a preferred solution is to use pure nickel, but with a thin underlying silicon layer. The effect of the silicon layer was reported to be a reduced carbon reduction at the interface [8] what practically is accompanied by the formation of a smoother contact layer, and in addition also a stable and low contact resistivity of $< 1 \times 10^{-6} \Omega \text{ cm}^2$ (see Fig. 3 and 4).

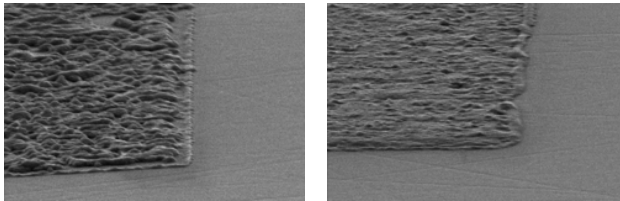


Figure 3: Morphology of Nickel-based contacts after high temperature annealing, left without and right picture using a thin silicon underlayer

For forming contacts to p-type layers, a first hurdle is to find a suited test method. Crucial is the high sheet resistance of p-type layers (because of low mobility and weak ionization), mainly if they are implanted. Our estimations show that values below $1 \times 10^{-4} \Omega \text{ cm}^2$ cannot be measured accurately because of the limitations coming from the underlying p-material. Nevertheless, commonly accepted is the use of aluminum in combination with titanium or nickel. Mostly stacked layers are reported, however, we found the optimum results regarding morphology and contact resistance using mixed layers of nickel and aluminum with a high content of aluminum (>30%, see also Fig. 5) [9].

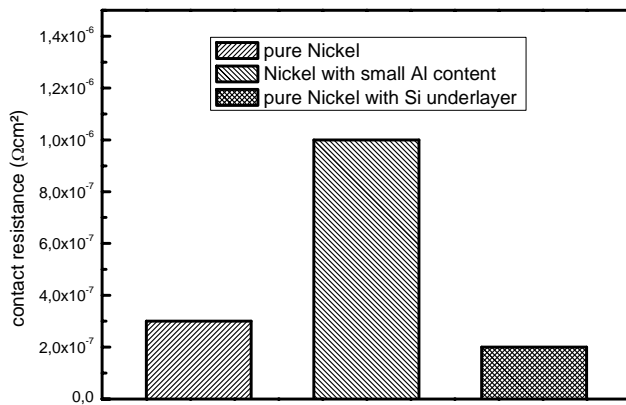
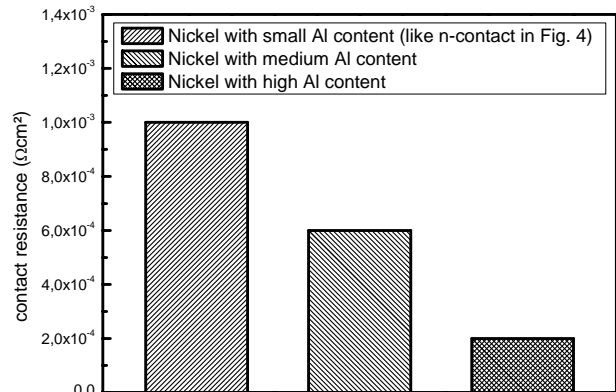


Figure 4: Typical contact resistance of different nickel based n-type SiC contacts, obtained from TLM measurements on highly doped n+-layers after a RTP sinter process at about 1000°C for 2 minutes

Additional challenges arise if neighboring n and p-type regions need to be ohmically contacted with preferable the same material. For this process we found best results if a mixture of nickel and aluminum with low aluminum content is used. The n-type contact is very good (see Fig. 4) and at the same time an acceptable p-type contact can be formed (see Fig. 5) what seems to be ideal for MOSFET structures,



e.g.

Figure 5: Typical contact resistance of different nickel based p-type SiC contacts, obtained from TLM measurements on highly doped p+-layers after a RTP sinter process at about 1000°C for 2 minutes

MOS INTERFACE

Also the formation of MOS capacitors as a basic element of MOSFETs reveals important differences to the established silicon devices. The most crucial problem today is of course the creation of an interface ending up with sufficiently high channel mobility in SiC power MOSFETs. A huge step forward was the use of nitrogen treatments by different variants, however, even if the now achievable specific on-resistances are quite close to the targets defined earlier, the resulting characteristics of SiC power MOSFET are still inferior compared to state of the art silicon power MOSFETs, mainly due to the weak transfer characteristics [10]. In addition, the effects of the incorporated nitrogen need to be investigated carefully, especially regarding the long term stability of the devices. This is still a focus topic of today's research work and is covered by numerous R&D programs worldwide. In the present paper a topic will be discussed which is strongly related to the complete process flow of a power MOSFET and is therefore not always evident during the analysis of a pure MOS capacitor.

Fig. 6 shows how a large positive oxide charge builds up in case of the use of polysilicon as a gate material instead of a simple metal.

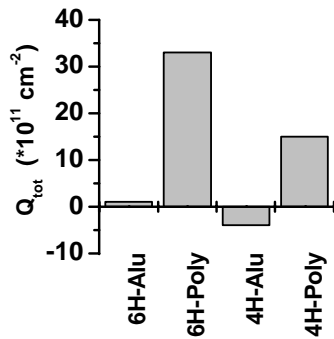


Figure 6: Oxide charge build up on MOS capacitors with polysilicon gate contacts compared to aluminum gated MOS devices, for 6H-SiC and 4H-SiC n-type

This charge built up is triggered by all high temperature processes following the deposition of the gate material (e.g. doping of the gate, contact annealing etc.).

For this problem, we found that the application of amorphous silicon can drastically reduce this positive oxide charge (see Fig. 7).

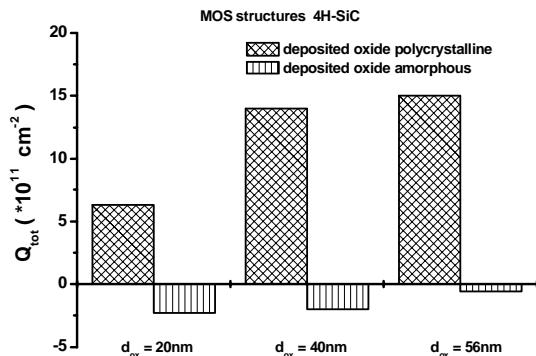


Figure 7: Influence of the structure of the silicon used as gate material (polycrystalline vs. amorphous)

We speculate that mechanical stresses are reduced in the case of an amorphous material. If the deposited layer contains already grain boundaries like in polysilicon, the further growth of the grains what is usually the results of heat treatments is suppressed while in an amorphous layer the formation takes part not before the first treatment. However, more analysis is required to get deeper into this issue. It should be mentioned at this point that even if the situation with the use of amorphous silicon is acceptable, still these MOS devices show higher positive charges than control structure using an aluminum gate instead of polysilicon.

CONCLUSIONS

Even if the technological processes for the fabrication of SiC power devices do not much differ from the well established silicon technology, important aspects remain which need the attention of device designers as well as of the technologist. Some of these topics were sketched in this paper, and especially the use of high temperature process steps was identified as the root cause for severe challenges within the device process flow. However, by using smart processes it is possible to handle these issues, and thus, even complex devices on the basis of silicon carbide can be fabricated. Open points remain and offer a large range of opportunities for future R&D regarding device design and fabrication technology.

ACKNOWLEDGEMENTS

The author would like to thank the people working on silicon carbide within SiCED, Infineon and Siemens. Their efforts and engagement was a decisive factor in order to be able to present these results. Some parts of the work are sponsored by the German Ministry of Education and Science.

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