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Process Modelling and Simulation for GaAs P-HEMT Gate Improvement and Control

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ABSTRACT

The drive to increase yield and volume of GaAs manufacturing has motivated the increased use of process and device modelling to understand and control sources of process variation and to improve device design for flexible manufacturing. Adapting tools and techniques developed for VLSI silicon, we have implemented a Technology CAD procedure for evaluation of process and device design. The purpose of this paper is to present results on how this procedure is being used to support our 150mm foundry upgrade, with specific focus on the L_g=0.2 micron Pseudomorphic HEMT process.

INTRODUCTION

Process and device modelling and simulation within the framework of Technology CAD (TCAD) is widely used in semiconductor silicon development and manufacturing to improve time-to-market, reduce cost and improve process and device design. Indeed, the recently published update to the international roadmap for semiconductors [1] declared an actual cost-reduction due to TCAD of 20% in 1999, and forecasts 35% for 2005. Although device modelling is widely reported in the III-V industry, see for example, [2], process modelling is, as yet, rather scarce. In this paper, we will show an example of how process modelling can be used to gain insight into technology options for gate processing in a double recess pseudomorphic GaAs HEMT (PHEMT) process, within a 150mm process line.

With the upgrade from 3 inch to 150mm GaAs wafer processing the issue of e-beam lithography wafer throughput becomes more critical, with photolithography potentially an attractive option. We have assessed three possible options for 0.2 micron gate processing within simulation: (A) pure direct-write e-beam lithography based upon our existing conventional tri-layer resist process [3]; (B) a mixed e-beam and optical lithography process (e.g. as in [4]); and (C) pure optical lithography using an i-line stepper (e.g. as in [5]). The process modelling contribution to this has been to assess process complexity and sensitivity, in particular the impact on gate CD control, and to provide quantitative guidelines and recommendations for initial process studies.

MODELLING AND SIMULATION

We have adapted commercial software tools used within the silicon industry for application to our GaAs PHEMT technology [6]. Typically process modelling is performed in a 2D vertical cross-section of the device, on the scale of the device (~10 micron) and aims to predict the device geometry, layer structure and topography, and doping distribution. In this work, we focus upon the device geometry and topography modelled through sequential deposition and etch stages. The specific processes modelled are metal evaporation, (PE)CVD nitride deposition, wet and dry (plasma) etch. The metal evaporation model has a narrow angular distribution of vapour flux impinging on the wafer surface with high sticking coefficient, giving rise to shadowing effects. In addition, we model a small component of isotropic deposition to simulate surface migration and/or re-emission. Nitride deposition is modelled as conformal (reactants have a low surface sticking coefficient). In this work, we are *not* attempting to explicitly model the lithography. Sophisticated equipment modelling software for both electron beam and photo-lithography is available (e.g. [7]) but requires accurate models for the resist exposure and development, which can only be obtained by detailed experimental calibration. Instead, for modelling of lithography, we have used typical resist profiles from SEM measurement and estimated the process control from observed variations.

GATE PROCESSING

Simulation of the metal evaporation deposition process into a direct write e-beam exposed tri-layer resist structure (process A) to create a mushroom (T-shape) gate is shown in figure 1 after lift-off stages. This has the desirable feature of a narrow gate stalk at the target gate length, with a wider cap for reduction of gate resistance. Total gate control of 3σ=10% is achieved with this process. Gate process option B

introduces a thin nitride layer prior to gate processing. The gate stalk is defined by e-beam lithography in a single thin resist followed by nitride etch and gate recess etch in the GaAs/AlGaAs layers. The wide (0.5µm) gate cap is then processed by (non self-aligned) optical lithography. Simulation is shown in figure 2 at gate deposition and after lift-off. This process has potentially greater critical dimension control of the gate stalk and throughput as compared to A. Process control may also be improved by the earlier nitride passivation of the surface in this process. Possible concerns are additional gate variation introduced by the nitride etch, increased parasitic capacitance (see later) and potential etch damage in the GaAs.

A fully optical lithography process with linewidth reduction by spacers has been advocated by the authors of [4]. Process modelling has investigated a possible process flow, C, to realise a 0.2µm gate. With careful control of humidity and resist thickness, a minimum line-width of 0.45µm can be routinely defined with an i-line stepper. In a conventional HEMT process, topography from the nearby source/drain metal lead to resist thickness non-uniformity in the source-drain gap and intolerable CD variation. These could be reduced by anti-reflection coatings, or by processing the ohmic contacts after the gate (necessitating a refractory metal gate). Reduction of the original optically defined aperture line-width can be achieved through the creation of inner spacers by conformal deposition and anisotropic etch of a nitride film (figure 3) leading to a possible device structure (figure 4) consistent with the SEM result shown in [2].

PROCESS SENSITIVITY ANALYSIS

We have used the simulation tools to guide a cost-benefit analysis of these three alternative gate processes. The purely optical lithography process C introduces additional sources of variation in the gate critical dimension (CD) control, due to the inner spacer process (variations in the deposited spacer material thickness and etch add to the original gate aperture variance). Estimates are shown in table 1 for different assumptions in these three steps: a worst-case 10% variance in each of these steps, gives a total gate control 3σ of 24% at 0.2µm. Better lithographic control is potentially achievable with optical enhancement techniques such as PSM.

For the mixed e-beam/optical gate process B, 2D device simulation [8] has been used to explore the effect of misalignment, giving rise to skew gates (schematically shown in figure 5), and the choice of gate stalk. In particular the parasitic contributions to C_{gs} and C_{gd} (see figure 6) from the fringing fields impact on the device gain. There is a trade-off between control of gate length and parasitic fringing field from the cap. At V_{ds}=2V the additional contribution to gate capacitance (C_{gs}+C_{gd}) variation from cap misalignment of 0.15µm is 6% for a stalk height of 0.10 µm. This should be compared to the effect of gate CD variation in the tri-layer process A, for which the stalk height is ~0.16 µm. A 10% variation in L_g gives an 8% variation in the total gate capacitance. Thus to get performance equal to process A at 2V, in process C we would need to control the gate length (combined e-beam lithography and nitride etch) variance to better than 8%, which implies that the e-beam process should aim to achieve 3σ=5%. In addition, the 0.1µm gate stalk gives rise to at least 6% higher mean gate capacitance than process A, implying that the target gate length should be reduced to achieve the same performance. Note also that the gate cap misalignment has different effects at low and high drain bias. At low bias, offsetting the gate cap to the drain side ("gamma gate" type structure) gives a reduction in C_{gs} and increase in C_{gd}. At high drain bias, C_{gs} increases due to the lateral extension of the depletion region on the drain side of the gate, which increases the effective channel length, giving rise to F_T degradation. To some extent this can be rectified by modifying the first recess geometry and GaAs cap doping, but at the expense of breakdown.

CONCLUSIONS

This paper has demonstrated the use of 2D process modelling in the study of three alternative gate processes. Although a purely optical lithography gate process, such as C, is attractive from throughput considerations, the gate control is likely to be worsened due to several contributing process steps, and the process is radically different from a conventional HEMT. From simulation, the combined e-beam stalk and optical gate cap process B looks promising for improving wafer throughput and gate length control. However, there is a trade-off between the control of the gate length and additional parasitic fringing field variance from the cap. To achieve the same performance and process control as a pure e-beam trilayer resist process A having 10% gate variation, would require a ~6% shorter gate length with 3σ control of better than 8%.

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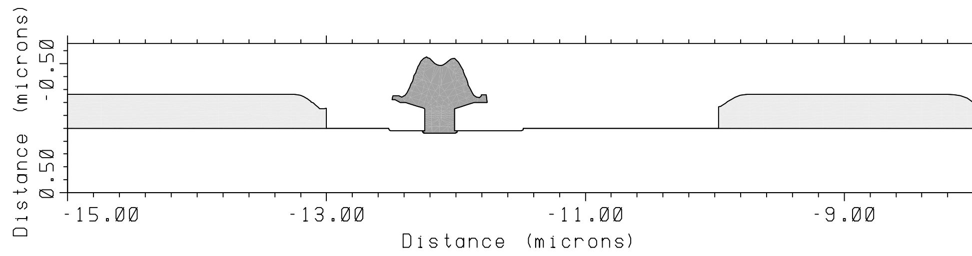

Figure 1 Simulation of Process A gate metal deposition (evaporation process) into a tri-layer resist mushroom gate structure shown after lift-off. (Results in this and figures 2 -4 were obtained with Avant! Taurus™-Topography and TSUPREM-4 software [6]).

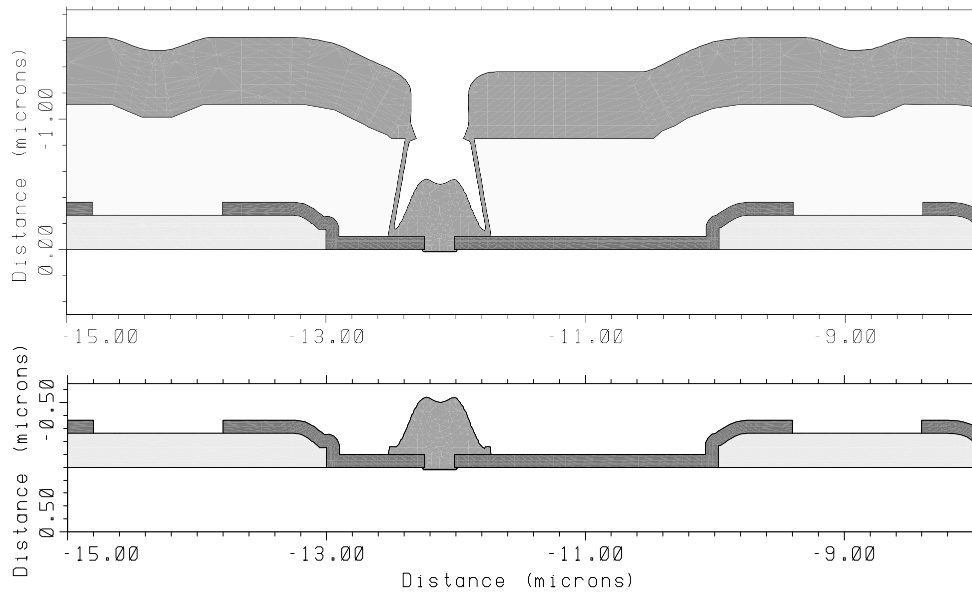

Figure 2 Simulation of Process B gate metal deposition (evaporation process) for an e-beam defined gate stalk window defined in a thin silicon nitride layer, with an optically defined gate cap, shown at gate deposition and after lift-off. The case of ideal alignment between cap and stalk is shown.

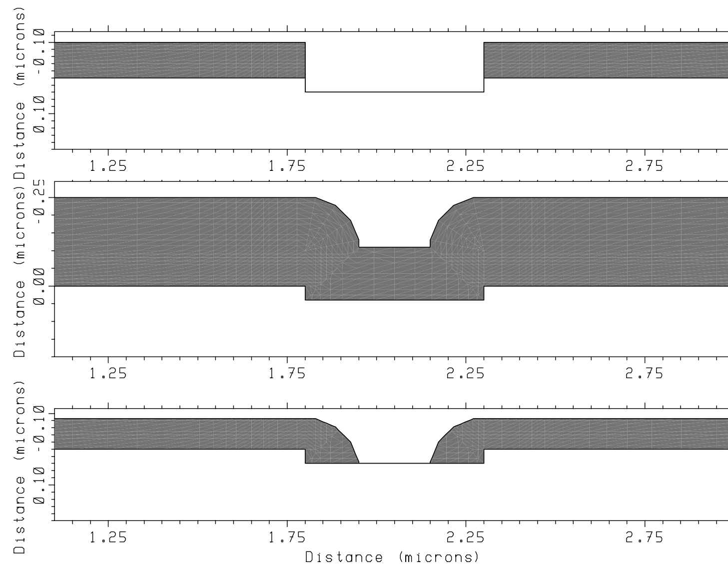

Figure 3 Simulation of Process C optically defined gate using line-width reduction process. An aperture of ~0.45 micron is defined in the GaAs cap; silicon nitride is used to form an inside spacer to reduce the aperture width.

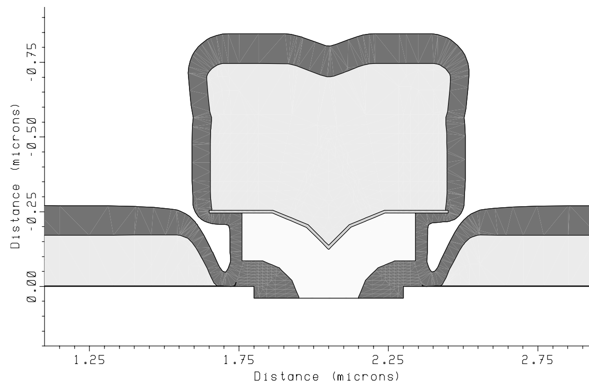

Figure 4 Simulated structure for a possible purely optical gate process with self-aligned ohmics (c.f figure 1 in [2]).

Initial 0.45µm aperture print feature control (3σ)	Nitride Spacer total control (3σ)	Final 0.2µm Gate Length Control (3σ)
± 0.045 µm (10%)	± 0.015 µm	± 0.047 µm (24%)
± 0.035 µm (7.8%)	± 0.015 µm	± 0.038 µm (19%)
± 0.035 µm (7.8%)	± 0.007 µm	± 0.035 µm (18%)
± 0.023 µm (5%)	± 0.007 µm	± 0.024 µm (12%)

Table 1 Estimated gate length control for the purely optical gate process C based on an initial i-line (365nm) aperture print of 0.45µm followed by a nitride sidewall deposition and etch to reduce the gate length to a nominal 0.20µm.

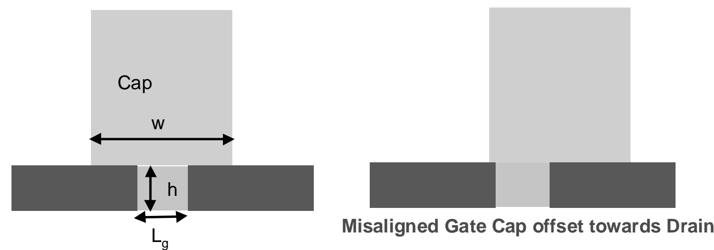

Figure 5 Schematic effects of misalignment of the gate cap and gate stalk for the mixed e-beam/optical lithography process B shown in Figure 2

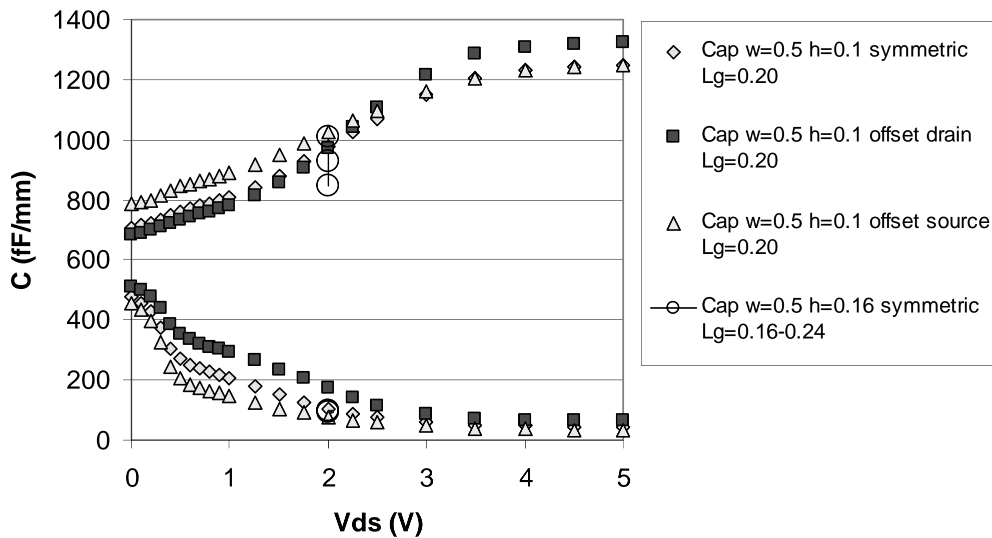

Figure 6 Modelled impact of misalignment in process B on the PHEMT Cgs and Cgd with a 0.5µm wide gate cap and a stalk height h=0.10µm for Lg=0.2µm as a function of Vds at Vgs=-0.3V. The effect of gate length variation 0.16-0.24 µm for a thicker stalk height of 0.16 µm with symmetric cap (process A) is also shown. (Simulation performed with Silvaco ATLAS-BLAZE™ software [8]).